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Influence of external mechanical stress on electrical properties of single-crystal n-3C-SiC/p-Si heterojunction diode

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This article reports for the first time the electrical properties of fabricated n-3C-SiC/p-Si heterojunction diodes under external mechanical stress in the [110] direction. An anisotype heterojunction diode of n-3C-SiC/p-Si was fabricated by depositing 3C-SiC onto the Si substrate by low-pressure chemical vapor deposition. The mechanical stress significantly affected the scaling current density of the heterojunction. The scaling current density increases with stress and is explained in terms of a band offset reduction at the SiC/Si interface under applied stress. A reduction in the barrier height across the junction owing to applied stress is also explained quantitatively. © 2015 The Japan Society of Applied Physics

Mechanical stress significantly affects the electrical properties of semiconductor devices. Under an applied stress, the band gap, carrier concentration, and carrier mobility in the semiconductor change, causing changes in the electrical properties of semiconductor devices.[1–3] The stress can be induced in the device during packaging or device processing, and it can be induced if the device is used in a mechanically challenging or harsh environment.[4] The piezoresistive, piezojunction, and piezo-Hall effects are the major phenomena related to the stress-induced changes in semiconductor devices.[1,5] These effects have been studied for years and are well established for silicon-based devices. The piezoresistive effect in Si has been used extensively to develop many stress–strain sensing applications.[6,7] The piezojunction effect in Si-based diodes and heterojunctions has been investigated for sensing and for device performance improvement.[1–3,8] The performance and reliability behaviors of strained silicon metal–oxide–semiconductor field-effect transistor devices have also been studied extensively.[9,10]

The SiC/Si heterojunction has been explored broadly as a promising candidate for various semiconductor device applications including high-frequency and high-voltage diodes, photovoltaic cells, and heterojunction bipolar transistors.[11–15] Further, 3C-SiC is a promising material for combination with Si because of its large band gap, good physical stability, and large electron mobility for high-temperature and high-power electronic devices.[16,17] The facility of readily growing 3C-SiC on large-diameter Si substrates gives it advantages over its counterpart materials. Therefore, the cost of using homoepitaxial films grown on 4H-SiC or 6H-SiC substrates is significantly reduced if 3C-SiC thin films grown on Si wafer substrates can be used.[18] Thus, it is very important to investigate the effect of stress on these heterojunctions.

The piezoresistive effect in 3C-SiC was recently investigated in our previous study.[19–21] We also reported the effect of mechanical stress on the electrical properties of the p-3C-SiC/p-Si heterojunction.[22] However, there are no studies on the effect of stress on the electrical properties of n-3C-SiC/p-Si heterojunctions. Therefore, in this letter we report the effect of mechanical stress on the electrical properties of n-3C-SiC/p-Si heterojunctions for the first time. The insight achieved in this study is not only important for understanding the device performance and effect of stresses induced during packaging but also shows the feasibility of using this device for stress sensing purposes.

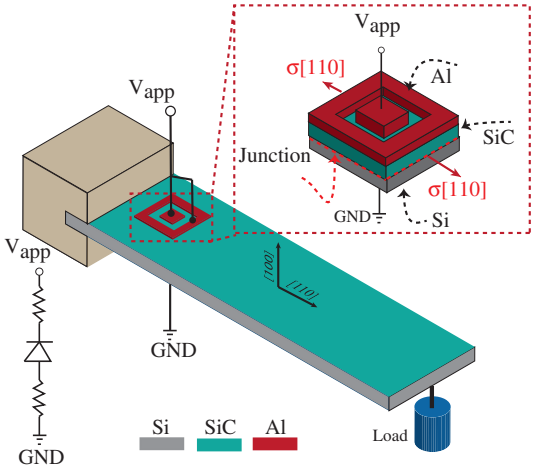

Fig. 1. Experimental setup for inducing stress in the heterojunction and *I–V* measurements with equivalent circuit diagram. σ[110] is the induced stress in the [110] direction.

The n-SiC/p-Si heterojunction diodes were fabricated by growing single-crystal n-type 3C-SiC to a thickness of 500 nm on p-type (100) silicon having a resistivity of 25 Ω cm in a hot wall chemical vapor deposition furnace at 1100 °C. The n-type doping concentration in the grown SiC, as determined by the hot probe method, was $(1–5) \times 10^{16}$ cm^{-3}. The surface of the SiC was cleaned using acetone, isopropanol, and then 1% HF before aluminum was deposited as an ohmic contact. The ohmic contacts on n-type SiC were patterned into an area of 500×230 μm^2 with a surrounding guard ring to reduce surface leakage currents. Aluminum was deposited as a back ohmic contact after the Si surface was cleaned and etched in HF solution. The Si wafer with the grown n-type SiC was diced into strips $32 \times 18 \times 0.625$ mm^3 in area for the application of mechanical stress by the bending beam method. Figure 1 shows the experimental setup. The X-ray diffraction (XRD) pattern of the deposited single-crystal 3C-SiC thin film is given in Fig. 2. The XRD pattern shows that 3C-SiC is grown epitaxially on the Si substrate. The inset of Fig. 2 is an image of the fabricated device showing the top Al contact and guard ring with the SiC layer under it.

Stress was induced in the heterojunction by the bending beam method, in which one end of the beam is fixed by a clamp, and the other end is bent by attaching different loads. The finite element method was used to obtain the magnitudes of the stress induced in the heterojunction. The method of

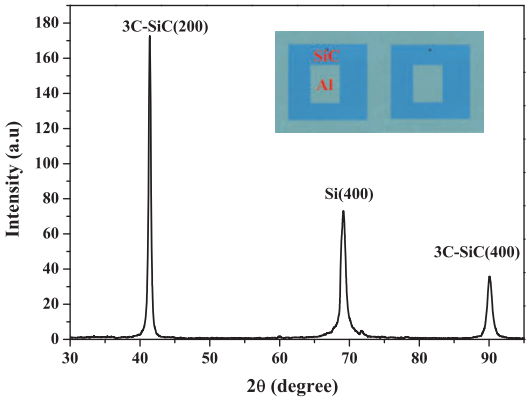

Fig. 2. XRD pattern of the grown 3C-SiC thin film on Si(100), showing that 3C-SiC is epitaxially grown on Si(100). Inset shows microscope image of the fabricated device.

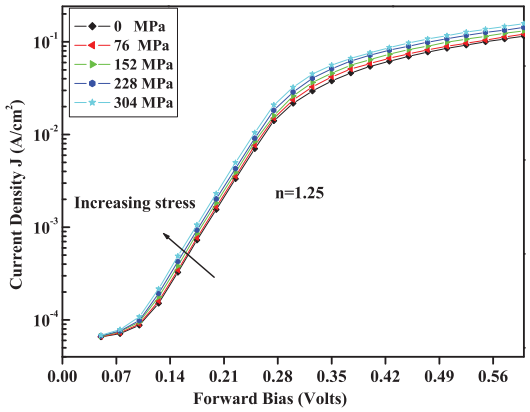

Fig. 3. *I–V* characteristics of the fabricated n-3C-SiC/p-Si heterojunction diode under various stress levels. Arrow shows the increasing trend of the heterojunction current with the applied stress.

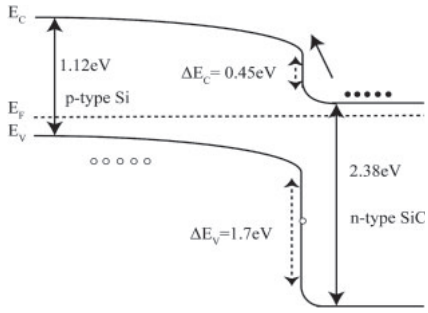

Fig. 4. Energy band diagram of the n-3C-SiC/p-Si heterojunction with band offset values from.[18)]

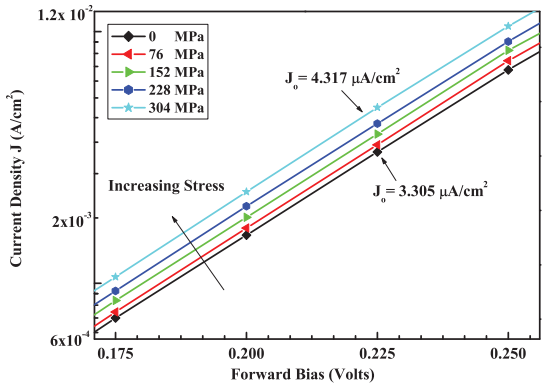

Fig. 5. Magnified plots of the *I–V* characteristics in the linear segment of the forward bias under various stress levels.

calculating the stress is described in detail in.[20)] Stresses from 0 to 304 MPa were induced by applying different loads at the free end of the SiC/Si beam. Figure 1 shows the experimental setup; the directions of the current and stress are indicated with respect to the orientation of the SiC/Si heterojunction. The current–voltage (*I–V*) measurements of the heterojunction were conducted using an Agilent U2722A source measure unit by sweeping the voltage from −2 to 0 V on the SiC side while the Si side was grounded.

Figure 3 shows the *I–V* curves of the n-SiC/p-Si heterojunction under various stresses. The forward bias current density in the heterojunction is given by the relation

$$J = J_0 \exp\left(\frac{qV_{\text{app}}}{nkT}\right), \tag{1}$$

where J_0 is the scaling current density, V_{app} is the applied voltage, q is the charge, n is the ideality factor, k is the Boltzmann constant, and T is the temperature. To understand the current mechanism in this heterojunction, the energy band diagram of the heterojunction is given in Fig. 4; the band offset values were taken from.[23)] The valence band offset in this heterojunction, $\Delta E_{\text{V}} = 1.7$ eV, is large enough to impede the flow of holes from Si to SiC, and the device current is thought to be due mostly to thermionic emission of electrons over a potential barrier.[14)] This potential barrier V_{B} can be expressed as[24)]

$$V_{\text{B}} = \Delta E_{\text{C}} + qV_{\text{bi}}, \tag{2}$$

where qV_{bi} is the part of the barrier due to bending of the energy levels, and ΔE_{C} is the conduction band energy offset. Figure 3 shows that the current in the linear segment of the forward current exhibited an increasing trend when the stress increased from 0 to 304 MPa. The ideality factors n for the unstressed and maximally stressed heterojunction were calculated and found to be the same. Therefore, the observed change in current in the linear segment of the forward current in Fig. 1 corresponds to an ideality factor of $n = 1.258$. It is well known that the ideality factor n is 1 when the diffusion current dominates and 2 when generation–recombination dominates.[24)] The ideality factor of 1.258 in our case indicates that the current in the heterojunction is dominated by diffusion and has a generation–recombination component, which is most likely to result from defects at the SiC/Si interface.

Figure 5 shows magnified plots of the linear segment of the forward current in the semi-log *I–V* data. The scaling current density J_0 of the heterojunction was calculated by extrapolating the linear segment of the semi-log curves to the zero-bias value. It has been observed that the scaling current density depends significantly on the applied external stress. The dependence of the scaling current density on the applied stress is shown in Fig. 6. It can be concluded that the scaling current density increases with applied stress from $J_0 = 3.305$ μA/cm^2 at 0 MPa to $J_0 = 4.317$ μA/cm^2 at 304 MPa.

When stress is induced in a semiconductor, the conduction band energy edge E_{C} is shifted from its unstressed value. The energy band edges are shifted in both Si and SiC.[25,26)] The conduction band edge shift under applied stress alters the energy band offset ΔE_{C} between Si and SiC in the hetero-

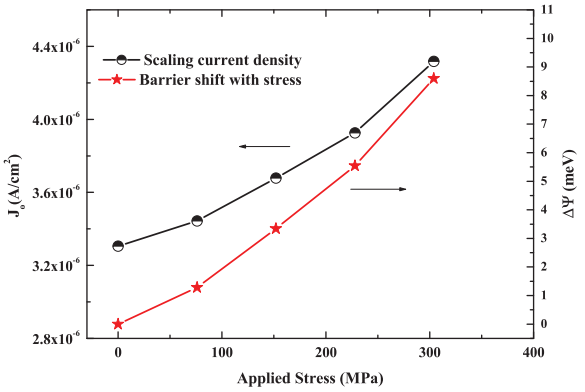

Fig. 6. Variation of scaling current density and barrier height shift in the heterojunction under applied stress.

junction. The edges can shift either in the same direction or in opposite directions depending on the crystal structure and direction of stress. As the 3C-SiC is grown epitaxially on Si, both of the materials are stressed under similar conditions; that is, the crystal plane is (100), and the applied stress is in the [110] direction for both of the materials, as shown in Fig. 1. In this particular case, the energy band edge E_C is reduced under applied stress in each material, but the amount by which the conduction band edge shifts is different in each material. As our results for the scaling current density show that the current density is increasing, we can conclude that the shift in the conduction band edges in the heterojunction reduces the conduction band offset ΔE_C between Si and SiC. This can be deduced from the exponential dependence of the scaling current density on the conduction band offset ΔE_C, which is given by the following relation:[20)]

$$J_0 \propto \exp\left(\frac{\Delta E_C}{nkT}\right). \tag{3}$$

As the potential barrier of height V_B is reduced owing to the reduction of ΔE_C, more electrons can have energies greater than the barrier height and can move to the conduction band from SiC to Si, resulting in an increase in the current across the barrier. The reduction of the barrier height, $\Delta\Psi$, due to the reduction in ΔE_C can be calculated using the following method. Let $J_0(0)$ be the scaling current density without stress and $J_0(\epsilon)$ be the scaling current density of the stressed heterojunction diode. Then the expressions for both current densities can be expressed using Eq. (3) as

$$J_0(0) \propto \exp\left(\frac{\Delta E_C}{nkT}\right), \tag{4}$$

$$J_0(\epsilon) \propto \exp\left(\frac{\Delta E_C + \Delta\Psi}{nkT}\right), \tag{5}$$

where $\Delta\Psi$ is the barrier height shift due to the induced stress. From Eqs. (4) and (5), the expression for $\Delta\Psi$ can be obtained as follows:

$$\Delta\Psi = nkT \times \ln\left[\frac{J_0(\epsilon)}{J_0(0)}\right] \tag{6}$$

The barrier shift calculated using Eq. (6) for different stresses is given in Fig. 6. The barrier shift increases from 1.28 to 8.6 meV when the stress is increased from 76 to 304 MPa.

In conclusion, the effect of external mechanical stress on the electrical properties of the n-3C-SiC/p-Si heterojunction diode was analyzed for the first time. The scaling current density in the heterojunction was observed to increase with increasing applied mechanical stress. The scaling current density increased from $J_0 = 3.305\,\mu A/cm^2$ at 0 MPa to $J_0 = 4.317\,\mu A/cm^2$ at 304 MPa. The increase in the scaling current density is a result of the reduction in the conduction band offset ΔE_C between n-3C-SiC and p-Si. The maximum reduction of 8.6 meV is observed under the maximum stress level of 304 MPa. These results show that the device performance can be significantly affected by stress in the [110] direction, and these effects must be taken into account for proper device performance. The results also show the strong feasibility of using this device for stress sensing applications.

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