Electrical Properties of p-type 3C-SiC/Si Heterojunction Diode Under Mechanical Stress

Afzaal Qamar, Philip Tanner, Dzung Viet Dao, Hoang-Phuong Phan, and Toan Dinh

***Abstract*— The current mechanism and effects of external transverse stress in the [110] orientation on the electrical properties of a single crystal (100) p-3C-SiC/p-Si heterojunction diode are reported for the first time. It has been observed that the current flow in the heterojunction is due to tunneling through the triangular potential barrier formed due to valence band offset between Si and SiC. The applied stress produces small changes in tunneling current when stress is increased from 0 to 308 MPa. The observed increase in current at 0.24 V is 10% at maximum stress of 308 MPa. The increase of tunneling current when applying stress is explained in terms of stress, which alters the out-of-plane effective mass, and the effective tunneling barrier height of holes in top subbands of p-type Si.**

***Index Terms*— p-type 3C-SiC/Si heterojunction, tunneling current, strain induced effects.**

I. Introduction

THE strain induced effects have been studied extensively in semiconductor devices due to its advantageous properties of subband modulation and piezoresistive effect [1]. In silicon (Si) based MEMS devices piezoresistive effect has been widely applied in mechanical sensors due to its large gauge factor [2], [3]. However, device applications at high temperature and pressure, intense vibration or corrosive environment limit the use of Si due to its lower energy band gap and mechanical properties [4]. Compared to Si, silicon carbide (SiC), with its large energy band, excellent mechanical properties, and good chemical inertness, is a promising material for applications used in harsh environments. SiC can be found in various polytypes 2H-SiC, 4H-SiC, 6H-SiC, 8H-SiC, and 3C-SiC [5], however, only the 4H-SiC, 6H-SiC, and 3C-SiC are reliable semiconductors in the industry [6]. The advantage of 3C–SiC polytype is that it can be readily grown on commercially available large diameter Si substrates. Therefore, the cost of using homo-epitaxial films grown on 4H–SiC or 6H–SiC substrates is significantly reduced if Si wafer is used for 3C-SiC thin films [7].

Under the application of stress, the energy bandgap of semiconductors will change, leading to a change in electrical properties. This effect has been deployed for stress/strain sensing applications known as the piezoresistive, piezojunction, and piezoHall effects. Piezoresistive effects in 3C-SiC have been reported recently in our study [8]–[10]. However, from the viewpoint of electronics device application, these effects cause unwanted errors and long-term instability in the electronic circuit. Therefore, there is a need to investigate the effect of stress on the performance of electronic devices. The stress can be incorporated into the semiconductor devices during the device fabrication process (e.g. wafer processing and packaging) and during applications in harsh conditions. For example high temperature can induce thermo-mechanical stress in the die due to the thermal expansion mismatch between the die and packaging materials. Mechanical impacts, deformation of the PCB (printed circuit board), high pressure, etc. can also create stress in the SiC/Si heterojunction [11]. It is important to know how the electrical properties of the junction are affected under stress.

Therefore, in this letter we investigate for the first time the current mechanism in the heterojunction and the effect of externally applied mechanical stress in the [110] orientation on p-type 3C-SiC/Si isotype heterojunction. This effect must be taken into account for circuit design and for harsh environment applications involving stress.

II. Device Fabrication and Setup

A 380nm thick p-type single crystalline 3C-SiC was grown on a p-type Si (100) substrate (which has a concentration of $N_a = 5 \times 10^{14}\text{cm}^{-3}$) by using a hot-wall LPCVD reactor at 1000 °C. Trimethyaluminium (TMAl) was used as the p-type dopant in the in-situ doping process. After the SiC was grown on Si substrate, the heterojunction of 200 μm $\times$ 500 μm area was defined by dry etching the SiC layer through to the Si substrate. The free carrier concentration of the SiC was measured by the Hall effect to be $1 \times 10^{18}\text{cm}^{-3}$. Al contacts were formed on top of the SiC and on the back of the Si substrate by photolithography and sputtering processes. The substrate was then diced to form a long strip of 60mm $\times$ 9mm $\times$ 0.625mm.

III. Results and Discussion

A. Current Mechanism of 3C-SiC/Si Heterojunction

Stress in [110] orientation was induced at the heterojunction by using the bending method in which one end of the SiC/Si beam was fixed, while the other end was bent by attaching different loads (Fig. 1(a)). The stresses induced to the SiC/Si heterojunction were obtained by using the finite element method (FEM). Accordingly, by varying the applied load at the free end of the SiC/Si beam, different stress

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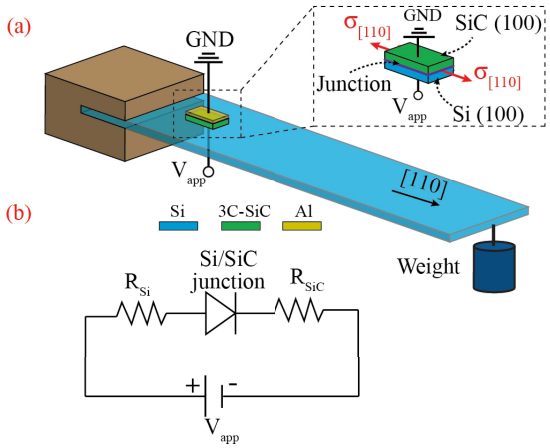

Fig. 1. Experimental setup for application of stress to the heterostructure (a), equivalent circuit diagram (b).

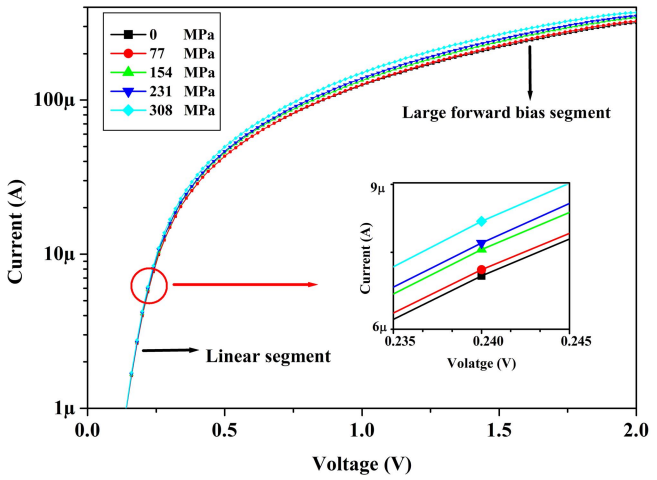

Fig. 2. I-V characteristics of p-type 3C-SiC/Si heterostructure diode under different amounts of applied stress.

magnitudes from 0 to 308 MPa were induced into the junction. The I-V curve of the SiC/Si heterojunction was measured by sweeping a positive voltage of 0∼2 V on the Si while the SiC was grounded. The equivalent circuit of the p-type 3C-SiC/Si heterojunction diode is shown in Fig.1 (b).

Fig. 2 shows the I-V characteristics of the single crystal p-3C-SiC/p-Si heterojunction diode under stress. The Fowler-Nordheim plots of the data in the linear segment are presented in Fig. 3. It is observed from the linear behavior of the Fowler-Nordheim plots that the current in the heterojunction is due to tunneling through the triangular potential barrier formed by the valence band offset between Si and SiC [12]. As positive voltage is applied to the Si with respect to SiC, holes accumulate on the Si side of the junction and tunnel through the triangular barrier (Fig4. (a)). The tunneling current can be expressed as a Fowler-Nordheim current as [13].

$$I = CE_s^2 \exp(-B/E_s) \tag{1}$$

$$I = CV_{app} \exp(-B/\sqrt{V_{app}}) \quad as\ E_s \propto \sqrt{V_{app}} \tag{2}$$

where pre-exponent C is a constant. The slope of the Fowler-Nordheim plot, B and electric field E_s are

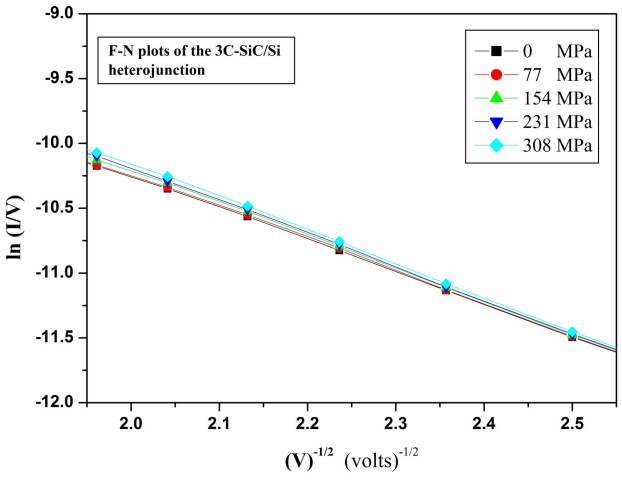

Fig. 3. Fowler-Nordheim plots of the heterojunction current.

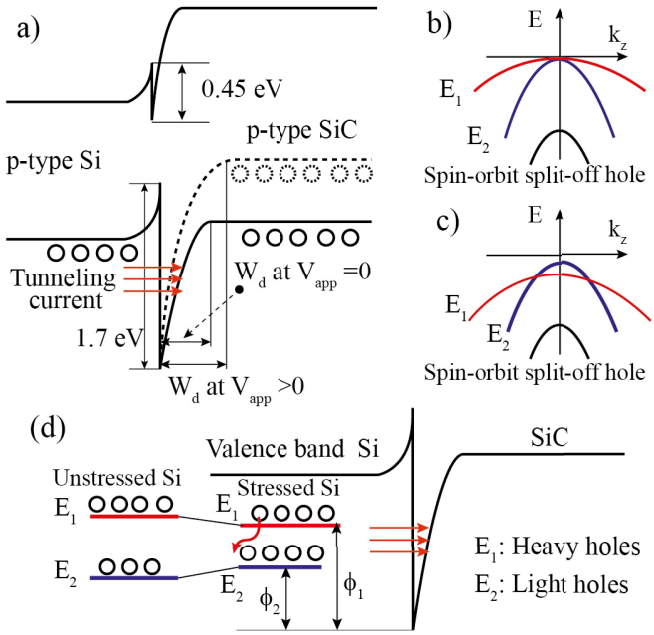

Fig. 4. Energy band diagram of p type 3C-SiC/Si heterostructure (a). Unstressed valence subbands of Si (b). Stressed valence subbands of Si (c). Hole repopulation in the top subbands and increase of tunneling(d) [15].

given by

$$B = \frac{8\pi}{3qh}\sqrt{2m^*\phi_o^3} \tag{3}$$

$$E_s = \frac{qN_A}{\varepsilon_s} \times W_d \tag{4}$$

$$W_d = \sqrt{\frac{2\varepsilon_s}{qN_A}(V_o + V_{app})} \tag{5}$$

where m^* is the tunneling effective mass, W_d is the barrier width, V_o is the barrier height between Si and SiC valence bands ($qV_o = \Delta E_v$) presented in electron volts (eV), V_{app} is the applied voltage, h is the Planck's constant and ϕ_o is the effective barrier height, ε_s is dielectric constant of SiC. Due to the band bending in the SiC at the junction, N_A is the total chemical concentration of Al in the SiC which was determined

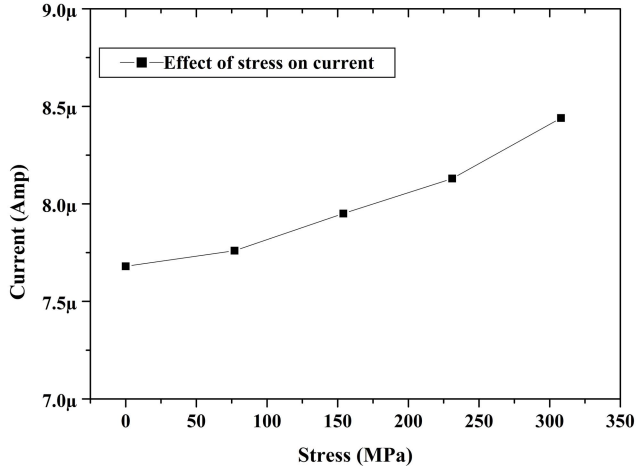

Fig. 5. Effect of stress on the heterojunction current in the linear segment of the I-V characteristics at 0.24 Volts.

to be 10^{20}cm^{-3} by secondary ion mass spectrometry (SIMS) analysis [14]. When the positive voltage is increased the barrier width will increase leading to the increase of electric field E_s and hence an increase in tunneling current (Eq.1).

B. Effect of Stress on Tunneling Current

When stress is induced to the p-type Si, the degeneracy is lifted and band warping occurs (Figs. 4b, c). The band splitting between two top subbands, (heavy hole and light hole), is reduced, and holes are repopulated from the higher energy subband (heavy hole) to the lower energy subband (light hole).

As the out-of-plane effective mass (perpendicular to the heterojunction plane) of holes in lower subband (light hole) is smaller than that in higher subband (heavy hole) i.e. $m^z_{E2} < m^z_{E1}$, so the resultant total effective mass decreases. Also the effective tunneling barrier height for the holes in subband E_2 (light hole) is smaller than the effective tunneling barrier height of holes in subband E_1 (heavy hole), i.e. $\phi_2 < \phi_1$ (Fig. 4(d)). Therefore, due to both reduced total effective mass and effective tunneling barrier height, the tunneling probability of holes through the barrier increases leading to an increase in tunneling current [15]. The contribution from the other subband (spin-orbit split-off hole) is neglected, because it is far away (0.44eV) from the band edge. The inset of Fig. 2 shows the zoom-in plot of the linear segment of *ln(I)* vs V_{app} and the increase in current at 0.24 V is given in Fig. 5. It is observed that the current is increased by 10% when stress is increased from 0 to 308 MPa. As the current in the large forward bias segment of the *ln(I)* vs V_{app} plot is dominated by the series resistance of the Si substrate, the increase in current in that segment is mainly due to the decrease of the resistance with applied stress in the p-Si substrate.

IV. Conclusion

The current mechanism and effect of stress on p-3C-SiC/p-Si heterojunction have been characterized for the first time in this letter. Fowler-Nordheim plots have been used to show that the current in the heterojunction is due to tunneling through the triangular potential barrier formed by valence band offset between SiC and Si. The applied transverse stress alters the hole population in the top two subbands in p-Si which results in a decrease in the out-of-plane effective mass and the effective barrier height of holes tunneling from Si to SiC. The tunneling current in the heterojunction increases by 10% as the stress is increased from 0 to 308MPa. Therefore, this increase of heterojunction current with applied stress should be taken into account for circuit design and for harsh environment applications involving stress.

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